VIGILANTE DATA HANDLING SYSTEM: ASIM FOR AUTOMATIC TARGET RECOGNITION

Nelson Alhambra
Jet Propulsion Laboratory
Pasadena, California

Steven C. Suddarth
Ballistic Missile Defense Organization
Washington, DC

Suraphol Udomkesmalee
Jet Propulsion Laboratory
Pasadena, California

ABSTRACT

VIGILANTE is an ultrafast smart sensor testbed for automatic target recognition (ATR) applications with a series of capability demonstration focused on a cruise missile defense (CMD) scenario. VIGILANTE's sensor/processor architecture is based on next-generation UV/visible/IR sensors and a tera-operations per second sugar-cube processor, as well as supporting airborne vehicle. This paper describes the data handling system portion of VIGILANTE and presents methodologies used for rapid prototyping and repackaging in a miniaturized form. Advanced techniques including 3D stacked subsystems are also addressed.

INTRODUCTION

VIGILANTE is a new sensing/processing architecture [1] comprised of the next-generation UV/visible/IR sensors and a high-speed, low-power sugarcube-sized processor. Vigilante offers hope of achieving a robust, real-time ATR system in a small package. Using the core computing engine developed under the BMDO's 3-dimensional artificial neural network (3DANN) program [2]-[3], 64 parallel convolution operations using up to a 64x64 kernel size can be carried out at tera-operations per second. This new processing possibility creates a large set of feature images from one raw image. These images are later fused to arrive at the final interpretation of the scene in real-time. VIGILANTE could interpret scenes with a thoroughness and speed, which is not feasible in conventional digital and optical processing.

The new, lightweight sensors are the Quantum Well Infrared Photodetector (QWIP), the Active Pixel Sensor (APS), and the delta-doped ultraviolet charge-coupled device (UV CCD). These three sensors cover the wavelength ranges 8 to 9, 0.5 to 0.9 and 0.3 to 0.7 μm, respectively. VIGILANTE's sensors can be queued to assist in the ATR functions of detection, classification, and precision tracking. For example, the UV wavelengths (0.3 to 0.7 μm) can be used for detection of plumes from BMDO targets of interest; IR (8 to 9 μm) is suitable for cold-body sensing and permits classification of these targets; and the visible wavelengths (0.5 to 0.9 μm) can be used for close-up tracking to provide aim-point selection for the end-game scenario. Eventually, the VIGILANTE sensors may be used for simultaneous fusion of the data from all wavelengths.

VIGILANTE will, for the first time ever, provide a complete multisensor and processing system in a small package that is suitable for ATR and pave the way for unique onboard, real-time processing of sensor images for autonomous interceptors and general-surveillance systems. Real-time target recognition will be demonstrated through a series of ground/airborne experiments using real target images.

SYSTEM DESCRIPTION

VIGILANTE consists of the Viewing Imager/Gimbaled Instrumentation Laboratory (VIGIL) and Analog Neural Three-dimensional processing Experiment (ANTE). VIGIL is an airborne telescope serving the dual functions of data acquisition for target recognition experiments and testing of novel active and passive focal plane imagers. The telescope will consist of a self-contained 15-cm Cassegrain unit, a gimbaled mirror, and channels for multiband sensors. A schematic diagram of the VIGILANTE system is shown in Figure 1.

ANTE is a prototype image-processing/target-recognition computer architecture based upon technology developed under the ongoing 3-dimensional artificial neural network (3DANN) program. 3DANN are a sugar-cube-sized, low-power neuroprocessor with its IC stack mated to an IR sensor array. ANTE uses a modified version of the 3DANN referred to as 3DANN-M (or commercially known as TeraCon). The special modifications to 3DANN allow VIGILANTE to accept data from any sensor of arbitrary size and format. More importantly, the 3DANN-M cube can be used for general image convolutions.

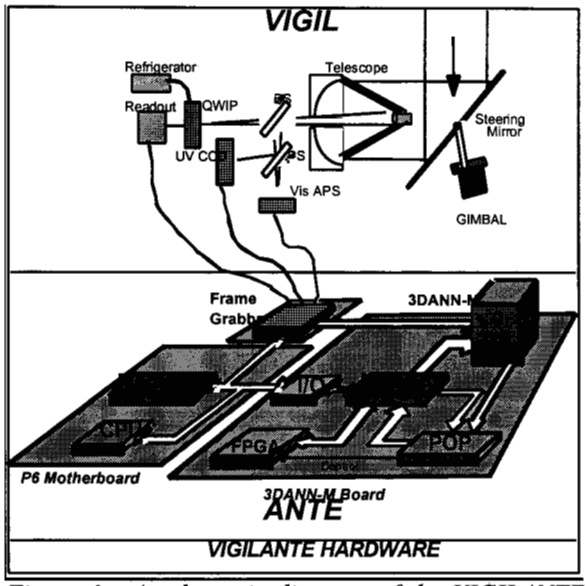

Figure 1. A schematic diagram of the VIGILANTE system. VIGIL is an integrated optical system that splits/transmits the incoming light (steered by a gimbaled mirror) detected by the respective IR/visible/UV sensors. ANTE is the processing system that selects each sensor channel for processing that is done by a commercial frame buffer and host processor and carries out real-time ATR by means of specialized, analog neural networks (3DANN-M) and a point operation processor (POP).

The general ATR process flow is depicted in Figure 2. A frame buffer holds the image and feeds a column or row of a 64x64 sub-window to CLIC every 250 ns. The 3DANN-M network then produces 64 inner-products (each with two 4096-element vectors) every 250 ns, thus accomplishing 64 convolutions of a 256x256 image with 64x64 masks in 16 ms. The 64 analog values generated by 3DANN-M are converted to 8-bit digital values and passed along to the Point Operation Processor (POP) for data fusion. Currently, the feedback memory and POP are implemented in four Adaptive Solutions' CNAPS array processor boards (each board containing 128 SIMD processors and 32 megabytes of memory)—providing flexibility to program different point operations. In the future, a custom VLSI implementation of POP may be designed and fabricated. POP takes the output from the 3DANN-M and performs the desired target recognition functions. Command and control of VIGILANTE operations are done though the P6 motherboard (shown as the processor/memory block in Figure 2).

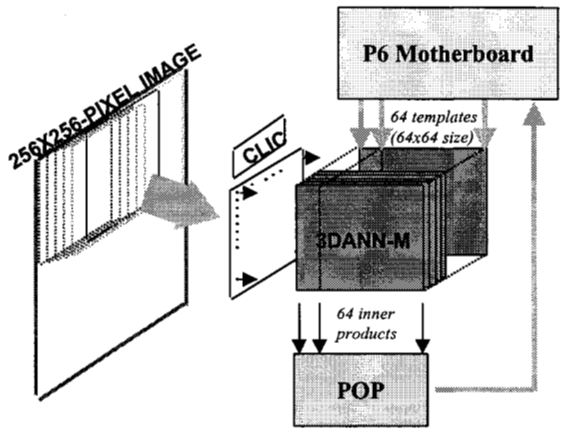

Figure 2. The VIGILANTE processing architecture that orchestrates the data flow from sensor through neural processor also serves as the basis for developing methodologies for ATR applications.

DATA HANDLING SYSTEM

VIGILANTE Data Handling System is a high-speed computer system capable of supporting the high bandwidth imaging and processing required for ATR applications, see Figure 3.

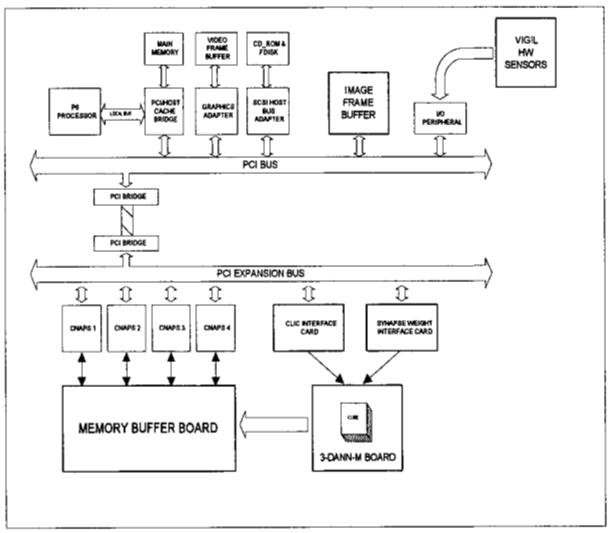

Figure 3. VIGILANTE Data Handling System manages data flow from sensors to 3DANN-M and POP. P6-based host computer, custom PCI interface cards, four CNAPS boards, and a memory buffer board comprise the system.

The system is a combination of a P6-based host computer on a PCI backplane and a PCI expansion chassis that contains the 3DANN-M sugarcube processor, custom high-speed PCI interface I/O

cards, four CNAPS boards, and a memory buffer board.

The image from VIGIL sensors is updated at 30 frames/sec (256x256 8-bit pixels frame) and stored in the frame grabber. The host processor, in concert with the CLIC interface card, transfers and formats the selected sensor image once every 250 ns. The formatting of data involves rearranging a raster version of the 256x256 image and storing it into 64-bit wide contiguous memory word locations. Every 250ns, a formatted 64-byte row or column image data is loaded into an array of 64x64 D-to-A converters internal to CLIC. The analog signals are then passed to the core inner-product computation engine of the 3DANN-M.

A set of 64 templates (64x64) can be simultaneously handled by 3DANN-M. The Synapse weight interface card stores five sets of templates and can load a set of 64 templates in 1 ms.

Analog outputs from 3DANN-M every 250 ms are digitized (8-bit resolution) and loaded into a memory buffer for CNAPS' POP processing. Closing the data loop, the host processor can evaluate results from CNAPS and setup scenarios for ATR—select a sensor input from the IR/vis/UV sensor suite, move particular sets of template in and out of 3DANN-M, provide the "context" for carrying out ATR functions (as it remembers which target is being tracked and updates tracking information), etc.

The current proof-of-concept implementation of the data handling system employs a full-size desktop power PC host and PCI expansion chassis connected with PCI bridge cards. The CLIC interface and synapse interface cards are the standard PCI card sizes and implemented using a AMCC PCI interface chip and Xilinx FPGAs for controller logic. 3DANN-M is mounted on a custom board (12x10 inches) that also consists of input buffer conditioners and output analog buffers with 32 dual-channel 8-bit A/D converters. Digitized outputs from 3DANN-M are stored in a large memory buffer board (12x10 inches). CNAPS boards are standard full-sized PCI cards.

FUTURE SYSTEM

In order to produce a deployable ATR system for small airborne vehicles, such as miniature interceptors, miniaturization of the data handling system can be realized using Multi-Chip Module (MCM) technologies. This Application-Specific-Integrated-Micro-instruments (ASIM) version of VIGILANTE will employ standard planner MCMs, Field Programmable MCMs, and advances in state-of-the-art, three-dimensional packaging technologies to dramatically increase data transfer rates and lower the volume and mass of this data handling system.

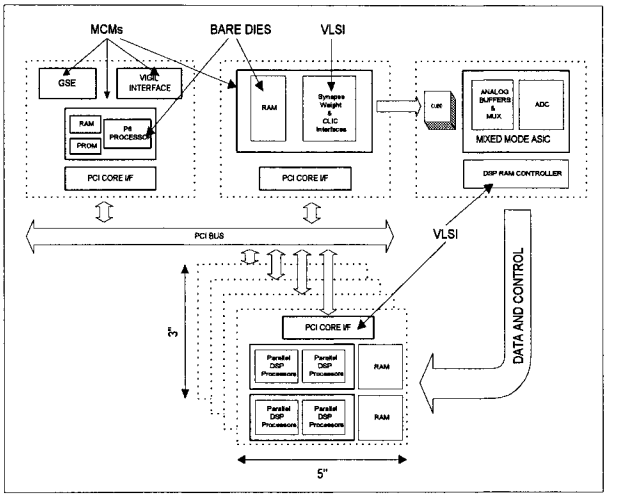

Figure 4. Future data handling system will take advantage of technology advances in MCM and 3D-packaging to produce a high-performance data handling system for VIGILANTE that is reduced in size, weight, and power consumption.

Figure 4 illustrates the similar architecture (see Figure 3) with MCM logical partitions. MCMs along with mixed-mode ASICs and custom VLSI are integrated on hybrid printed circuit boards (3"x5"). Three-dimensional system packaging, with high-density I/O on all four sides, including the PCI-Bus will enhance data transfer rates and reduce the overall volume. Multi-DSP processors replace the current CNAPS implementation of POP processing. The next generation of the VIGILANTE data handling system will incorporate this new design and provide a practical, ultrafast microsystem of ATR that literally fits on top of the human hand.

CONCLUSIONS

VIGILANTE establishes unique system architecture for ATR. Its data handling system orchestrates the data flow from sensors to 3DANN-M, POP, and host computer. The proof-of-concept hardware has been completed, and the future system will employ MCM technologies to provide deployable micro-systems (ASIM) that serve our nation's NMD and TMD needs.

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